10/075121 02/13/02

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U.S. **UTILITY** Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10075121	02/13/2002	710	305	~~2181~~ 2112	~~Wong~~ PATEL

**APPLICANTS: Bolt Thomas; Moon William;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		Q02-1031-US1
Verified and Acknowledged Examiners's intials			

TITLE : Use of the universal serial bus as an internal architecture within IDE disk array

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid	Primary Examiner	Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAMER	PREPARED FOR ISSUE	Application Examiner	

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